1.(Cancelled)

2.(Cancelled)

3.(Cancelled)

4.(Currently Amended) A filter comprising a plurality of interconnected modular basic units, and a delay line equipped with takeoff points to furnish delayed sampling values (x1, ..., xN; xi) of a digital signal (x), such that the delay times of the sampling values are integer multiples n of the period with n = 0, 1, 2, 3, ... of a sampling clock pulse coupled to the digital signal (x),

each basic unit contains a programmable weighting device, a linkage device, and a delay device, which delays the data conducted to it by a single period (T) of the sampling clock pulse or by a simple integer multiple thereof, and

the filter further contains a programmable control device, which switches over or switches off a part, especially half, of the data inputs of the basic unit to achieve forward and/or backward filtering and/or sign inversion and/or a change of the active filter length,

wherein ~~The filter of claim 3, characterized in that~~ the programmable control device comprises a sign inverter, which, in dependence on a third control signal (I), inverts the signs of the data values passed through it, which are conducted to the associated data inputs of the interconnected modular basic units, and said programmable control device further comprises a second switching device, which, in dependence on a second control signal (P), switches into an ineffective state a last stage (N) of the delay line and/or a data input.

5.(Original) The filter of claim 4, characterized in that the programmable weighting device comprises a multiplier, to whose first input a coefficient (c) is conducted and to whose second input a data value to be weighted is conducted, the coefficient (c) being programmable and being stored in a register.

6.(Original) The filter of claim 5, characterized in that the linkage device comprises a first adder, whose first and second input is coupled to a first and second data input of the basic unit, and whose output is coupled to the second input of the multiplier.

7.(Original) The filter of claim 6, characterized in that the respective first data input of the modular interconnected basic units are supplied with the delayed sampling values (x1, ..., xN) in sequential time order, and the respective second data inputs are supplied essentially uniformly with a single data value, which is coupled to the delay line, when the first switching device is in a first switch position (F1), and is coupled to at least one data output of the modular interconnected basic units, when said first switching device is in a second switching position (F0).

8.(Original) The filter of claim 7, characterized in that the linkage device comprises a second adder, whose first and second input are coupled to a third data input of the basic unit and to the output of the multiplier, and whose output is coupled to the input of the delay device, the third data input being used to accept an output data value of the preceding basic unit, and the output of the delay line being connected to a data output of the basic unit.

9.(Original) The filter of claim 8, characterized in that the registers of the modular interconnected basic units are linked to one another like a shift register through a coefficient input and a coefficient output, so as to write the coefficients (c) serially into the registers.

10.(Original) The filter of claim 9, characterized in that the number of existing functional units in the basic units, especially at the beginning and/or end of the modular interconnected basic units, is reduced, whereby modified basic units result.

11.(New) A programmable digital filter that receives an input signal x[N] and provides a programmable digital filter output signal, said programmable digital filter comprising:

a first basic unit that receives and sums said input signal x[N] with said programmable digital filter output signal, and multiplies the resultant sum with a first coefficient signal value C_N that is stored in a first memory element and provides a product that is input into a first delay of one period, wherein said first delay provides a first basic unit output signal;

a second basic unit that receives and sums a past value input signal x[N-2] with said programmable digital filter output signal and multiplies the resultant sum with a second coefficient value C_{N-1} that is stored in a second memory element to provide a product that is summed with said first basic unit output signal and this resultant sum is input to a second delay of one period, wherein said second delay provides a second basic unit output signal;

a third basic unit that receives and multiplies a past value input signal x[N-4] with a third coefficient value C_{N-2} that is stored in a third memory element to provide a product that is

summed with said second basic unit output signal and the resultant sum is output as said programmable digital filter output signal;

a control processor that adaptively provides said first, second and third coefficient values; and

a sign inverter, responsive to a first control signal from said control processor, for selectively inverting the sign of said programmable digital filter output signal that is fed back to said first basic unit and said second basic unit.

12.(New) The programmable digital filter of claim 11, wherein said first and second memory elements are located in a common memory device.

13.(New) The programmable digital filter of claim 11, wherein said programmable digital filter is located on a integrated circuit.

14.(New) A programmable digital filter that receives an input signal x[N] and provides a programmable digital filter output signal, said programmable digital filter comprising:

a delay line having a plurality of delays, wherein said delay line receives said input signal x[N] and provides a past value input signal x[N-2] and a past value input signal x[N-4];

a first basic unit that receives and sums said input signal x[N] with said past value input signal x[N-4], and multiplies the resultant sum with a first coefficient signal value C_N that is stored in a first memory element and provides a product that is input into a first delay of one period, wherein said first delay provides a first basic unit output signal;

a second basic unit that receives and sums said past value input signal x[N-2] with said past value input signal x[N-4] and multiplies the resultant sum with a second coefficient value C_{N-1} that is stored in a second memory element to provide a product that is summed with said first basic unit output signal and this resultant sum is input to a second delay of one period, wherein said second delay provides a second basic unit output signal;

a third basic unit that receives and multiplies said past value input signal x[N-4] with a third coefficient value C_{N-2} that is stored in a third memory element to provide a product that is summed with said second basic unit output signal and the resultant sum is output as said programmable digital filter output signal;

a control processor that adaptively provides said first, second and third coefficient values; and

a sign inverter, responsive to a first control signal from said control processor, for selectively inverting the sign of said programmable digital filter output signal that is fed back to said first basic unit and said second basic unit.

15.(New) The programmable digital filter of claim 14, wherein said first and second memory elements are located in a common memory device.

16.(New) The programmable digital filter of claim 14, wherein said programmable digital filter is located on a integrated circuit.